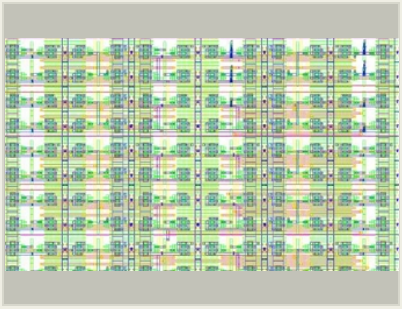
Radiation Hardened High Speed Integrated Circuits Double Data Rate I/O for Extreme Operating Environments, Phase I

Completed Technology Project (2017 - 2017)

Project Introduction

Manned and robotic space missions require high-performance electronic control systems capable of operating for extended periods in harsh environments that are subject to radiation, extreme temperatures, vibration and shock. Semiconductor technologies capable of meeting these demanding requirements tend to have limited capabilities, are expensive, and are not easily configured for specific mission requirements. Leading-edge applications will benefit from the ability to implement high speed interconnect protocols between host processors and system slaves, such as sensors, actuators, power managers, imagers and transceivers. The development of a Radiation Hardened Double Data Rate (DDR) embedded macro is proposed for insertion into digital integrated circuits (ICs) suitable for scalable single and multi-core processors, special purpose logic functions and scalable memory blocks on a space-qualified, radiation hardened integrated circuit digital fabric. A NASA-funded Structured ASIC architecture is under development at Micro-RDC, capable of meeting space-grade requirements while creating a cost-effective, quick-turn development environment. The SASIC fabric will implement known Radiation-Hardened-By-Design (RHBD) techniques on an advanced 32nm Silicon on Insulator (SOI) CMOS process, supporting high-density, high-speed low-power implementations. A unique Master Tile architecture with through-seal-ring connections allows the designer to define dedicated logic functions, scalable memory blocks and user-defined I/Os; all on a single, scalable integrated circuit. The 32nm SOI CMOS process technology platform incorporates RHBD building-blocks (e.g. flip-flops, gates, distributed memory, block memory, I/O) required for the systems designer to implement functional blocks for application-specific requirements. During this project, key blocks for a DDR3 macro will be specified and evaluated for optimum inclusion into the Micro-RDC SASIC.



Radiation Hardened High Speed Integrated Circuits Double Data Rate I/O for Extreme Operating Environments, Phase I Briefing Chart Image

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Small Business Innovation Research/Small Business Tech Transfer

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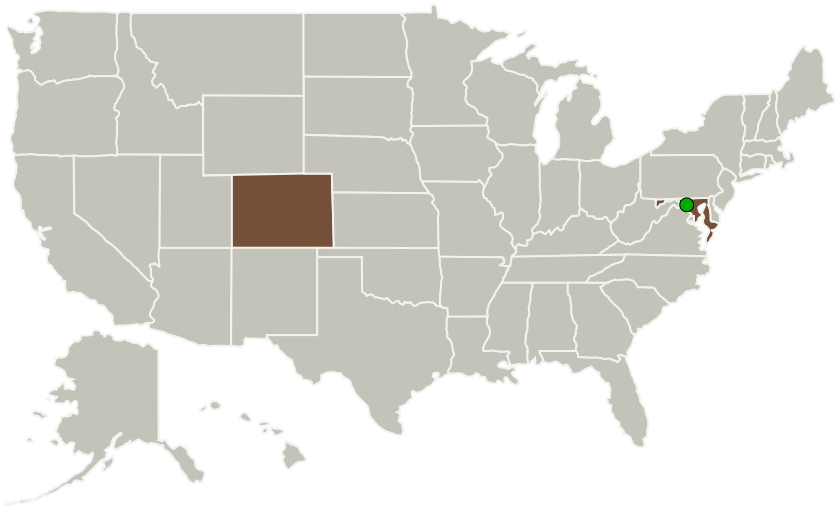
Primary U.S. Work Locations and Key Partners



Organizations Performing Work	Role	Type	Location
Microelectronics Research Development Corporation	Lead Organization	Industry	Colorado Springs, Colorado
Goddard Space Flight Center(GSFC)	Supporting Organization	NASA Center	Greenbelt, Maryland

Primary U.S. Work Locations	
Colorado	Maryland

Project Transitions

June 2017: Project Start

December 2017: Closed out

Closeout Documentation:

- Final Summary Chart*(https://techport.nasa.gov/file/140820)*

Organizational Responsibility

Responsible Mission Directorate:

Space Technology Mission Directorate (STMD)

Lead Organization:

Microelectronics Research Development Corporation

Responsible Program:

Small Business Innovation Research/Small Business Tech Transfer

Project Management

Program Director:

Jason L Kessler

Program Manager:

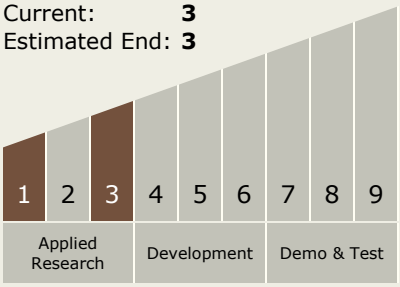
Carlos Torrez

Principal Investigator:

Greg Pauls

Technology Maturity (TRL)

Start: **1**
Current: **3**
Estimated End: **3**



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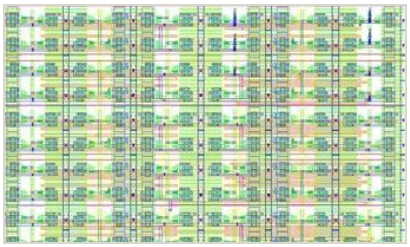
Images



Briefing Chart Image
Radiation Hardened High Speed Integrated Circuits Double Data Rate I/O for Extreme Operating Environments, Phase I Briefing Chart Image
(https://techport.nasa.gov/image/135659)

Technology Areas

Primary:

- TX02 Flight Computing and Avionics
  - TX02.1 Avionics Component Technologies
    - TX02.1.1 Radiation Hardened Extreme Environment Components and Implementations

Target Destinations

The Sun, Earth, The Moon, Mars, Others Inside the Solar System, Outside the Solar System